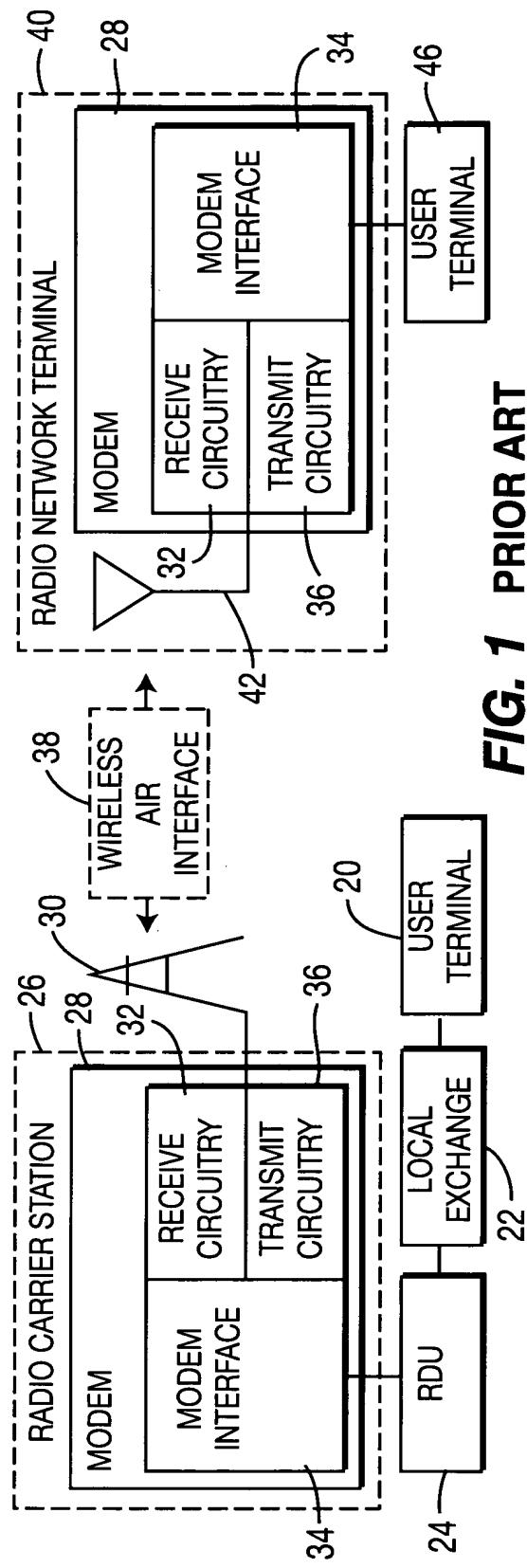
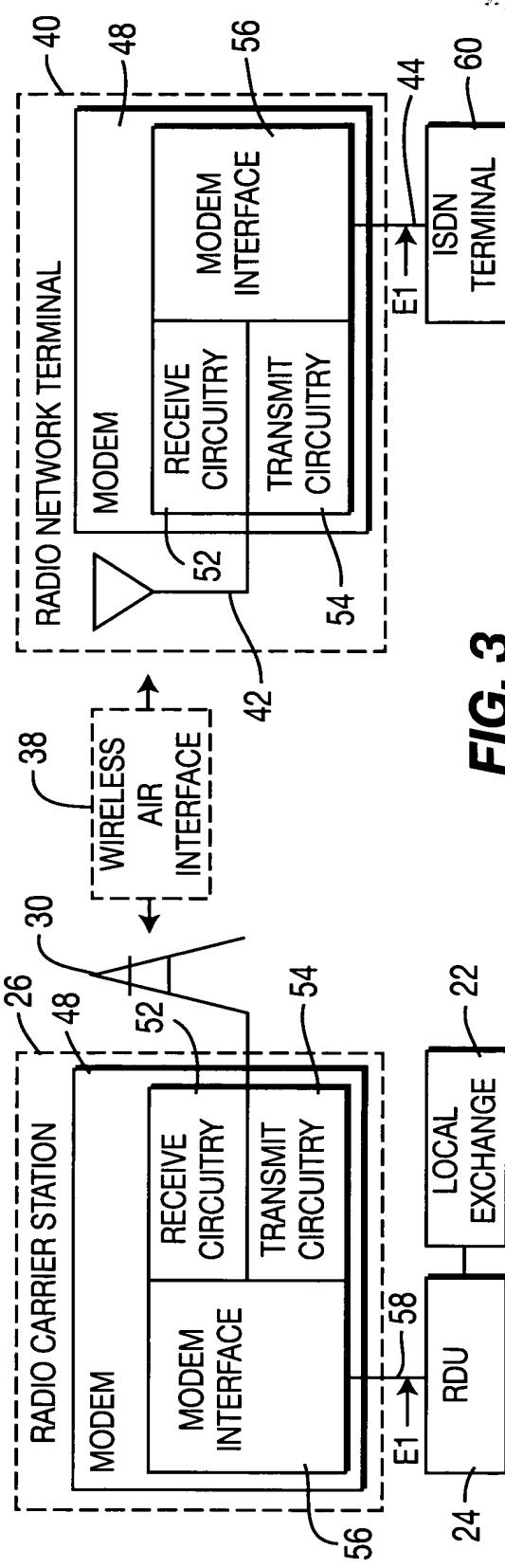
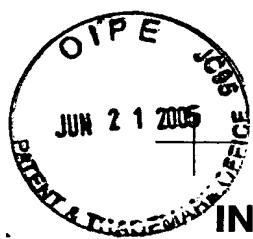


JUN 21 2005



1/3





# MODEM INTERFACE-TSI BLOCK

2/3

**FIG. 2**

**FIG. 2A** | **FIG. 2B**

This block diagram illustrates the architecture of a digital communication system, showing the flow of data between various components and the structure of the backplane slots.

**PCM/IOM Block:** This block contains the **PCM HWY IN** and **PCM HWY OUT** ports, connected to the **PCM/IOM** module. The **PCM HWY IN** port is connected to the **PCM/IOM** module via line 56. The **PCM HWY OUT** port is connected to the **PCM/IOM** module via line 62. The **PCM/IOM** module is connected to the **I/O** module via line 64.

**I/O Block:** The **I/O** module is connected to the **PCM/IOM** module via line 64. It is also connected to the **HDLC 1**, **HDLC 2**, and **HDLC 3** modules via lines 1141, 1142, and 1143 respectively. The **I/O** module is also connected to the **ARM** module via line 88.

**HDLC Modules:** The **HDLC 1**, **HDLC 2**, and **HDLC 3** modules are connected to the **PCM/IOM** module via lines 1081, 1082, and 1083 respectively. They are also connected to the **ARM** module via lines 1001, 1021, and 1041 respectively. Each HDLC module is connected to a **HR** (Half-Rate) block via lines 1081, 1082, and 1083.

**ARM Block:** The **ARM** module is connected to the **I/O** module via line 88. It is also connected to the **HDLC 1**, **HDLC 2**, and **HDLC 3** modules via lines 1001, 1021, and 1041 respectively. The **ARM** module is connected to the **API** module via line 140.

**API Block:** The **API** module is connected to the **ARM** module via line 140. It is also connected to the **IOM INTERRUPT** module via line 98.

**DSP Block:** The **DSP** module is connected to the **ARM** module via line 78. It is also connected to the **IOM INTERRUPT** module via line 140.

**Backplane Structure:** The backplane is organized into several slots:

- HWY3:TS0-2:** 72<sub>n-2</sub> (top), 72<sub>n-1</sub> (top), 72<sub>n</sub> (top), 70<sub>n-2</sub> (middle), 70<sub>n-1</sub> (middle), 70<sub>n</sub> (middle).
- 9 HDLC SLOTS:** 110<sub>1</sub> (top), 110<sub>2</sub> (middle), 110<sub>3</sub> (bottom).
- 3 ARMSLOTS (HWY3:TS9-11):** 106<sub>1</sub> (top), 106<sub>n</sub> (middle), 100<sub>n</sub> (bottom).
- 8 IOM SLOTS (HWY2:TS8-15):** 96<sub>1</sub> (top), 96<sub>n</sub> (middle), 90<sub>n</sub> (bottom).
- 8 DSP SLOTS (HWY2:TS0-7):** 84<sub>1</sub> (top), 84<sub>n</sub> (middle), 80<sub>n</sub> (bottom).
- 3 INTERNAL PCM HWYS:** 86<sub>n</sub> (top), 82<sub>n</sub> (middle), 80<sub>n</sub> (bottom).

Each slot is connected to the **IOM INTERRUPT** module via lines 92<sub>1</sub> through 92<sub>n</sub>, 94<sub>1</sub> through 94<sub>n</sub>, 84<sub>1</sub> through 84<sub>n</sub>, 86<sub>n</sub>, and 82<sub>n</sub> respectively. Each slot is also connected to a **BR** (Byte-Rate) block via lines 92<sub>1</sub> through 92<sub>n</sub>, 94<sub>1</sub> through 94<sub>n</sub>, 84<sub>1</sub> through 84<sub>n</sub>, 86<sub>n</sub>, and 82<sub>n</sub> respectively. Each **BR** block is connected to a **R** (Rate) block via lines 90<sub>1</sub> through 90<sub>n</sub>, 80<sub>1</sub> through 80<sub>n</sub>, 86<sub>n</sub>, and 82<sub>n</sub> respectively. Each **R** block is connected to a **W** (Word) block via lines 106<sub>1</sub> through 106<sub>n</sub>, 100<sub>1</sub> through 100<sub>n</sub>, 104<sub>n</sub>, 102<sub>n</sub>, and 100<sub>n</sub> respectively.

**FIG. 2A**

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3/3

56

## MODEM INTERFACE-TSI BLOCK

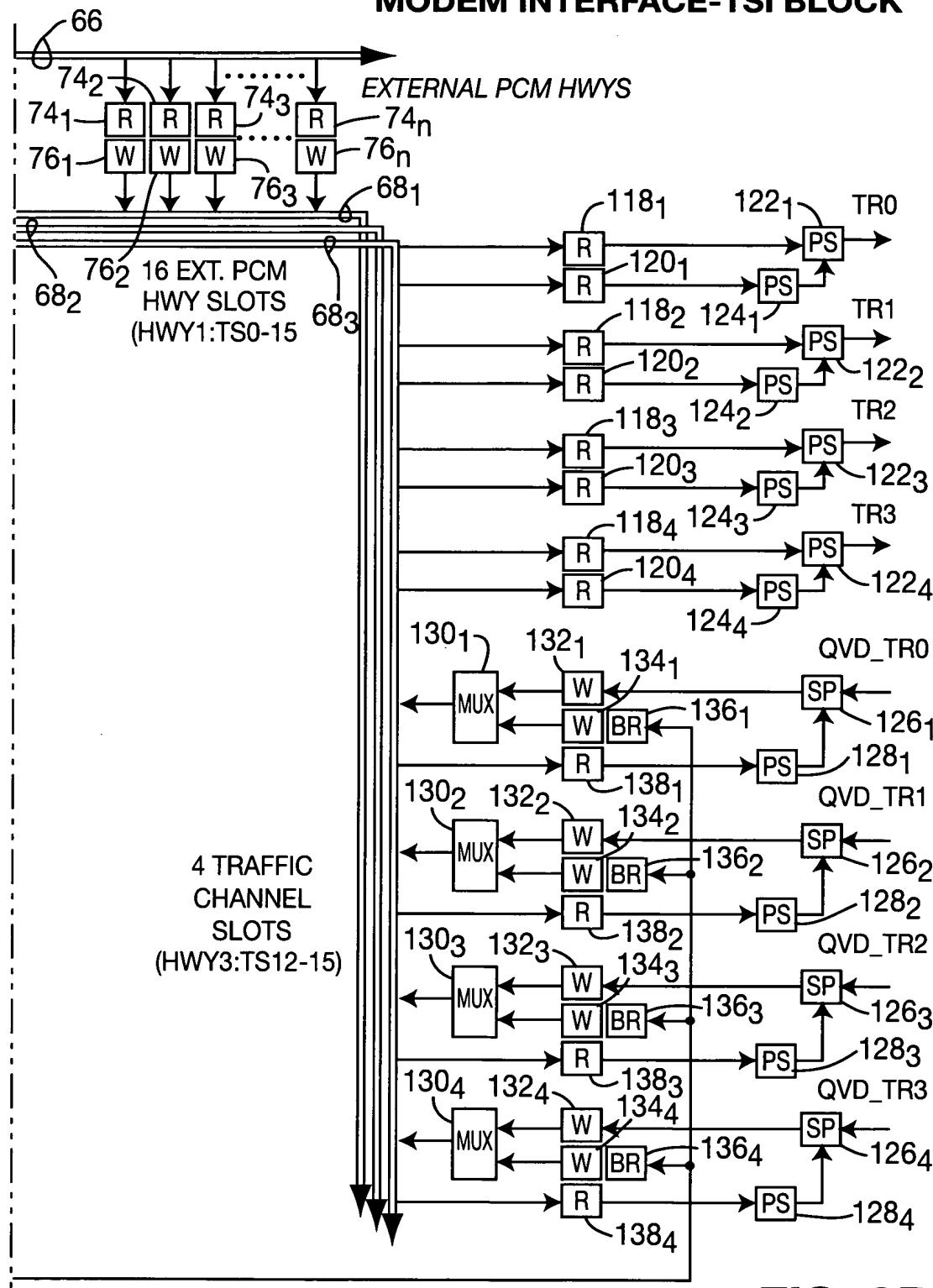


FIG. 2B

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